Investigation of a new low cost and low consumption single poly-silicon memory

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Abstract

In this paper is presented an investigation on a new low cost and voltage consumption single poly-silicon memory cell for passive **RFID** (**R**adio **F**requency **ID**entification)applications. This structure is low cost due to its single poly-silicon design. This memory cell has two particularities : the first one is that no deported capacitor is necessary to program this cell which allows to reduce the structure size to 1.1µm². The second one is the way the cell is erased. A Zener diode is used to generate carriers in order to be injected into the floating gate. This Zener diode is one of the key points for the functionality that has to be validated with some electrical trials. These trials permit to integrate and use the Zener diodes measured in simulations of the complete memory cell. This is done to validate the best candidate between the Zener diodes used for the cell and highlight the efficiency in consumption and rapidity to erase the cell. Besides, the writing and the reading cases are simulated in order to show the low consumption required by the cell during these phases.

Keyword : Single poly-silicon memory, low cost, low consumption, Zener effect.

1. Introduction

Most of the **N**on-**V**olatile **M**emories (**NVM**) found in low cost and consumption applications, such as **RFID** tags, are single poly silicon memories [1-7]. They are usually made in **L**ogic **NVM** (single poly silicon **NVM** without mask added) [6-7] to reduce the cost. Nevertheless, these NVM have several disadvantages such as: high potentials or a combination of positive and negative polarizations and important die size. In this paper, a new low cost and voltage consumption single poly-silicon memory cell is presented. The cell does not necessitate a deported capacitor compared to the existing single poly used for the **RFID** memories [5-7] that reduce the size of one structure.

This memory is programmed (Writing/Erasing) using low and strictly positive polarizations. This point is important because the architecture does not require a charge pumping to generate the negative polarisation. This allows to reduce the consumption of the chip because charge pumping used 90% of the energy necessary by the chip during the programming operations [17]. The structure cost is reduced as it is made in **CMOS** (**C**omplementary **M**etal **O**xide **S**ilicon) standard logic process [6].

2. Presentation of the device structure

A schematic, layout and a cross section of a new single poly-silicon EEPROM are shown in fig.1.

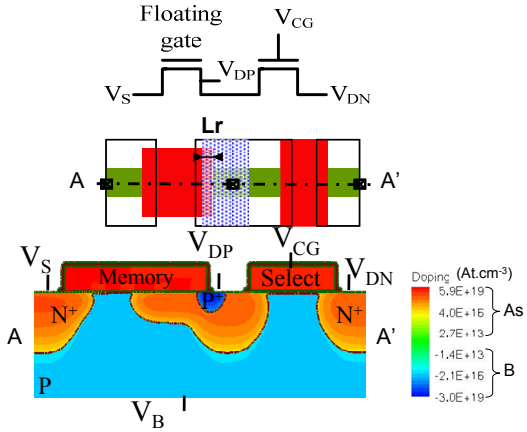

Fig. 1: (a) Layout, (b) schematic and (c) cross section of a TCAD process simulation of the new single-poly cell double implant

The memory and select transistors have a uniform 7nm oxide giving way to a simplified production process. Two main differences between this memory cell and a classical single poly-silicon memory cell are observed. The first disparity is a P^+ implant which is performed into the N^+ drain implant of the memory cell to form a Zener diode. The aim of this diode is to generate carriers in order to erase the structure with a low voltage consumption. The second disparity is that a deported capacitor is unnecessary to program the cell, thus reducing the structure size under 1.1µm² for a

0.13µm technology node. Nevertheless, suppressing the deported capacitor means that the structure has to be well designed to obtain the right coupling ratio to write and erase the cell.

The most interesting **LNVM** have a size which range from 5µm² to 65µm² [10-16]. The second is a P^+ implant which is performed into the N^+ drain implant of the memory cell [10-11]. The size gain, compared to all these memories, is at least 5 times better for the technology node.

3. Process flow of the structure

The fabrication of the structure is summarized in fig. 2.

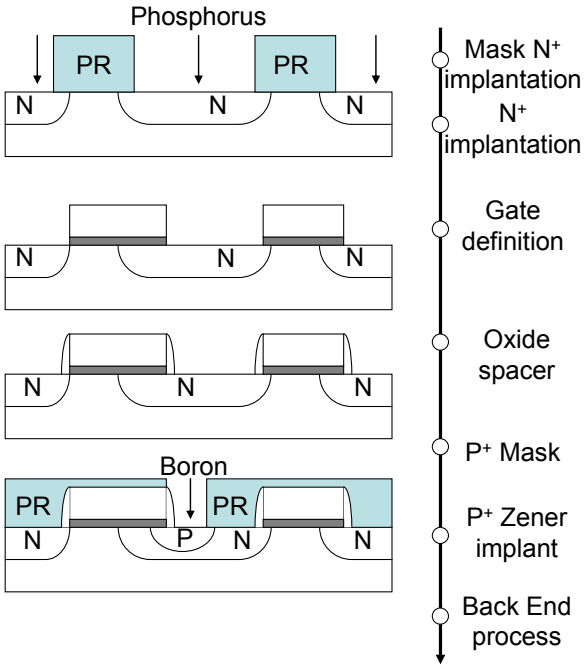

Fig. 2 : Process flow of the new single-poly cell double implant

First of all, an implantation of Phosphorus is used with a mask of photoresist employed to hide the zone not implanted. The dose employed for this implantation is 0.5x cm^{-2} (x is the reference dose) and an energy at 3y KeV (y is the reference energy). This step is followed by an uniform oxide growth of 7nm for the select and the memory transistor and a deposition of the gate. Furthermore, an oxide spacer is done and the photoresist is deposited to implant the P^+ zone to form the Zener diode. This operation is achieved with the same step than PMOS transistor implantation to avoid a specific layer in order to reduce the fabrication cost. The P^+ zone is implanted with Boron at a dose of 3x cm^{-2} for an energy at 1y KeV. After this step, the process fabrication continues its flow towards the back end process.

4. Programming and reading concepts

To program this memory cell, two methods are used : the Zener effect [7], [11] to erase and the Fowler-Nordheim mechanism [8], [9] to write.

The Zener or tunnel effect is employed to generate electrons by the P^+/N^+ junction (fig.3). This phenomenom occurred for a sufficient polarization (Vj) applied on the diode. When Vj is sufficient, the band bending becomes such that some electrons can tunnel from the valence band (Ev) to the conduction band (Ec). Under the electric field (ξ) applied on the space charge, the electrons are accelerated and can generate electron-hole pairs under a sufficient electric field by impact ionization or avalanche effect.

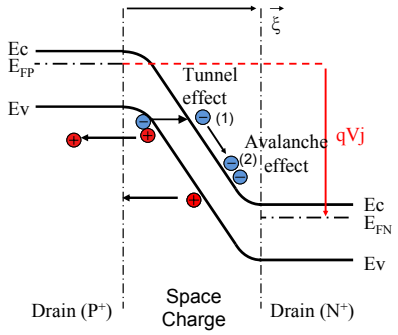

Fig. 3 : Tunnel and avalanche effect on a diode

These carriers generated under the gate to drain overlap can be, if they are sufficiently energetic, injected into the floating gate (Erasing fig.4).

The necessary voltages applied for the erasing operation are 5V on V_{DN} and V_S contacts at the same time, while V_{DP} contact is grounded. These voltages allow to increase the polarizations on the floating gate, by coupling. This gives a sufficient field for the carriers generated by the Zener diode, on the oxide region, to be injected into the floating gate.

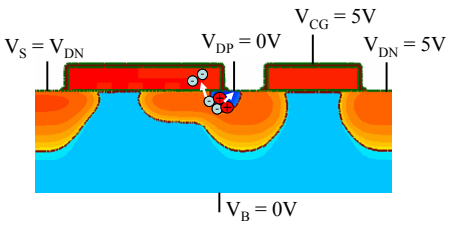

Fig. 4 : Erasing of the new single-poly cell double implant by a Zener effect

The well-known Fowler-Nordheim phenomenon is employed to remove these electrons on the source side (writing fig.5) by applying a voltage of 9V on the source while the other contacts are floating.

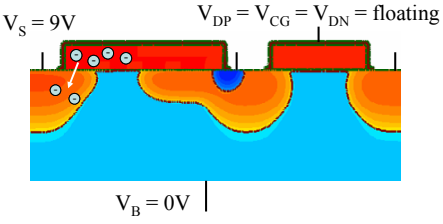

Fig. 5 : Writing of the new single-poly cell double implant by the Fowler Nordheim effect

The memory cell can be read when both drain contacts are grounded and a positive polarization must be applied on the source. The polarizations applied on the structure are summarized in Table I.

	Write	Erase	Read
V_{DN} (V)	Float	5	0
V_{DP} (V)	Float	0	0
V_S (V)	9	5	0.2
V_{GC} (V)	0	5	2

Table I: Programming potentials of the new single-poly cell double implant

5. Array memory of the cell

The memory array for this structure is designed with an EEPROM NOR architecture. The choice of this array is to facilitate the access of one memory cell by using a select transistor. An example of a four cells array with the new single-poly cell double implant can be seen in fig.3.

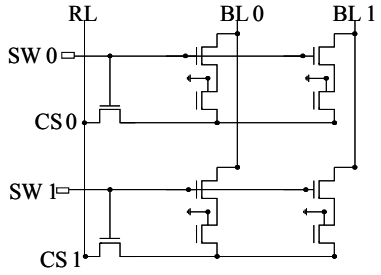

Fig.6 : Array of 4 new single-poly cells double implant

This array is easily achieved because the contact V_{DP} is always grounded no matter which operation is done on the memory. The V_S contacts of the structures are common that allow writing by byte. And for the erasing case, each cell could be erased bit by bit.

6. Investigations on the Zener diode

To achieve this structure, an investigation was done to find the optimum Zener diode. The requirements targeted are that there is no voltage variation in temperature with the Zener breakdown and no addition of mask. The three diodes choices are represented with the following split :

Diode	1	2	3
P doping	Boron	Boron	Boron
Dose	1x	2x	3x
Energy	1y KeV	1y KeV	1y KeV

For the three diodes tested, the N^+ implant is the same. The specie used is Phosphorus at a dose of 0.5x cm^{-2} for an energy of 3y KeV.

On these diodes, the measures are made on two different temperatures (25°C and 125°C) and the results obtained are shown in fig.6.

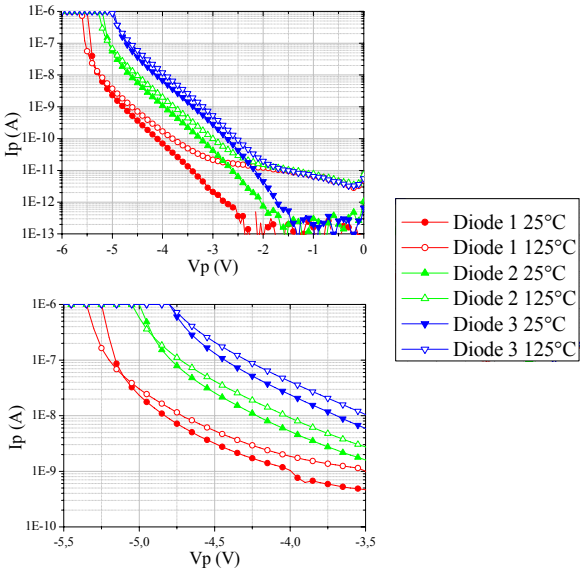

Fig. 7 : (a) Electrical characterizations of Zener diodes and zoom on breakdown temperature shift at 1µA (b) Zoom on the current curves around the Zener to Avalanche effect transition

As represented in fig.7, the variation of the diodes voltage breakdown ranges from 0 to 0.1V for a temperature variation ranging from 25 to 125°C at 1µA (fig.7).

The leakage current obtained for the three diodes, for a low voltage, is stronger at 125°C. This is due to the reduction of the diodes band gap with temperature. Furthermore, it is visible in this figure that the current for the three diodes is a contribution of two phenomenons: the Zener effect and the avalanche effect. For the three diodes, ranging from 0 to -4.9V, the Zener current is the predominant one. The currents at ambient temperature are lower than those measured at a higher temperature. As the Zener current increases with the temperature, this explains why under 5.3V for diode 1, 5.1 V for diode 2 and 4.9V for diode 3, this current is induced by the Zener effect.

Moreover beyond these voltages the current is attributed, for the three diodes, to an avalanche effect which delays the increase of the current. Nevertheless, the shift obtained for the three diodes do not exceed 0.1V. This is possible thanks to the two effects combined together where a consequent shift on the breakdown voltage is avoided, with a fixed current of 1µA.

According to these results, some process trials are made on the memory structure by inserting these Zener diodes in the fabrication flow. In parallel to these trials, a process comparison is made between the results obtained by the Sentaurus TCAD simulator with a STMicroelectronics standard process and the process trials (fig.8). The diode 3 is used for this comparison.

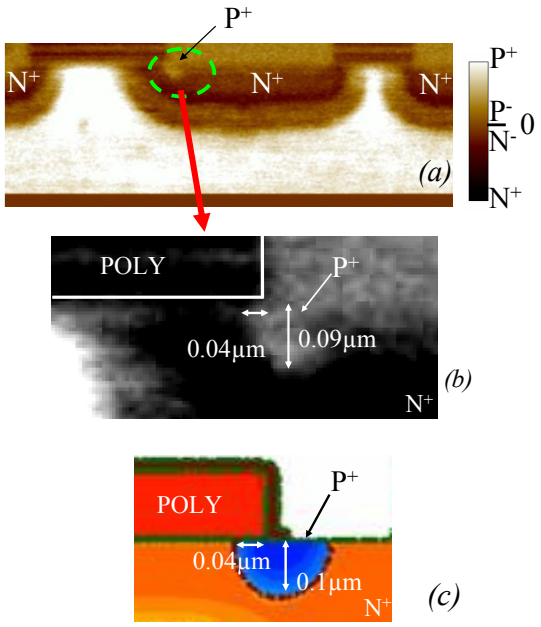

Fig. 8 : (a) AFM SCM cut and (b) zoom on the poly-silicon overlap of the P^+ implant (c) TCAD process simulation of the double implant

The process trials are analyzed with an **A**tomic **F**orce **M**icroscopy **S**canning **C**apacitance **M**icroscopes (**AFM SCM**) analysis. These results, obtained from the **AFM SCM**, allow to monitor the P^+ implant. This insures that the implantations profile results in the process flow correspond to the simulations results. In accordance with the results in fig.8, the **AFM SCM** cut gives a positive match to the simulation results. The diffusion of the P^+ implant in the process simulation is the one obtained in the process flow.

7. The new single-poly cell double implant TCAD simulations

In accordance with these process simulations, the programming of the memory is simulated by using TCAD Sentaurus simulator. The simulations for the Zener effect are done for the different diodes giving way to various diffusion lengths Lr (fig.1.b) under the gate. The results, which represents the charge into floating gate (Q_{FG}) and the gate current (I_G) versus programming time for the erasing case, are shown in fig.6.

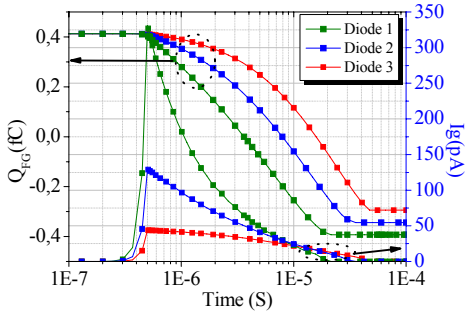

Fig. 9 : Cell erasing Qfg(time) and Ig(time) for the different diodes implantations

Table II underlines the impact on the variation of the charge injected into the floating gate (ΔQ_{FG}) in agreement to the process diode used.

Diode	1	2	3
Lr (nm)	40	70	90
Time (µs)	20	30	40
ΔQ_{FG} (fC)	0.82	0.75	0.68

Table II: Results of ΔQ_{FG} for the different diodes

As seen in Table II, to improve the charges injection efficiency, the diffusion of the P^+ implant (Lr) must be as small as possible. This is explained by two factors. The first one is that the doping gradient is reduced when the P^+ diffusion length increases for the identical N^+ implant. The second factor is that the coupling ratio induced by the capacity between the overlap of the drain N and the gate is reduced when the P^+ implant diffusion becomes more important under the gate. The field is diminished and it becomes less favourable for the carriers to be injected. The optimum Zener diode for this memory is an overlap of Lr = 0.04µm which corresponds to a ΔQ_{FG} = 0.82fC. In addition, the cell pulse must run for 20µs.

No matter which diode is used to write the cell, the pulse must last 1ms for a charge quantity injected of 0.8fC (fig.10).

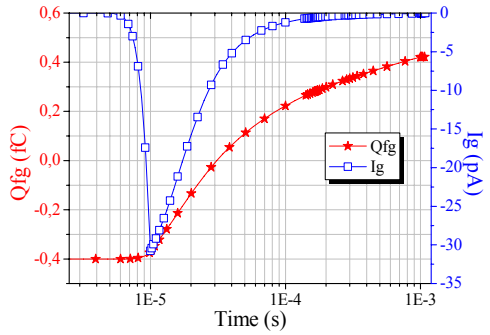

Fig. 10: Cell writing Q_{FG}(time) and I_G(time) for diode 1

These results induce a good overlap which is taken between the source implant and the gate. When this overlap is increased, the coupling ratio diminishes leading to an unfavourable electric field applied on the oxide to inject carriers.

When the cell programming is achieved, two states of charge are obtained. The results obtained from simulations are the following (fig.11).

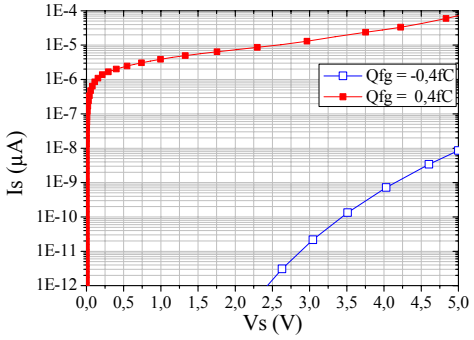

Fig. 11: Cell reading $I_S(V_S)$ with $|Q_{FG}|$=0.4fC

The polarization summarized in table I is applied on the structure. To differentiate the erase from the write state, for a read current fixed at 1µA, a source polarization of 0.2V is sufficient

Table III summaries all the results obtained for the programming operation of the structure.

	Pulse	Voltage	Current consumption
Write	1 ms	9V	5 nA
Erase	20 µs	5V	1 µA

Table III: Programming results for diode 1

The current necessary to write the cell is very low where a few nano-amps are sufficient for 9V. For the erasing, only 5V are applied on the structure for a current of only 1 µA during 20µs. In order to distinguish the two states, only 0.2V are required for a reading done at 1 µA. In comparison, to the CMOS logic process memories (**LNVM**) [10-16], the polarizations required range from 5 to 19V for a few milliseconds.

8. Conclusions

The structure presented in this paper is entirely simulated on TCAD simulators ranging from the process to the electrical results. The Zener effect, governed by the diffusion and dose of P+ implant into the drain N^+, is controlled and optimized by electrical characterizations on different diodes. This characterization put forth the weak variation in temperature of the diode breakdown voltage. The diode choices have been integrated to achieve the process flow of the memory cell in order to be compared with AFMs SCM analysis. The electrical results simulated are promising, a 5V polarization is sufficient to erase the cell for a short erasing time of only 20µs. The size of this structure is under 1µm² for a 0.13µm technology node which is really small for a memory using a Logic process. Only low and strictly positive polarizations are necessary to program the cell, which is not the case for all logic memories that require positive and negative voltage [12-16]. This allows to reduce the consumption and the surface occupied by the charge pumping.

All the results obtained for this new single poly-silicon memory are encouraging and they meet the requirements to be integrated in RFID applications.

9. References

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