# Experimental Validation of the DSTATCOM Based on SiC-MOSFET Multilevel Converter for Reactive Power Compensation

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## ABSTRACT

Power quality problems are associated, among other things, with the reactive power generated at the AC side in distribution systems. In this regard, the three-phase distribution static compensator is actually becomes a viable alternative in order to achieve reactive power compensation or in other words to obtain a unity power factor. This paper introduces the experimental validation of the distribution static compensator based on a 7-level cascade H-Bridge converter. The experimental test bench is based on the silicon carbide metal-oxide-semiconductor field-effect transistor devices. The results are obtained by using a fixed switching frequency model-based predictive controller based on a pulse-width modulation strategy. The proposed design is implemented to mitigate power quality issues induced by reactive load and experimental results are provided to show the performance of the proposed controller.

**Keywords:** Predictive control, active power filter, cascaded H-Bridge multilevel converter, reactive power compensation.

## NOMENCLATURE

| | |
|---|---|
| CPDs | Custom power devices. |
| DSTATCOM | Distribution static compensation. |
| DVR | Dynamic voltage restorer. |
| CHB | Cascade H-Bridge. |
| MPC | Model predictive control. |
| THD | Total harmonic distortion. |
| $C_{\rm dc}$ | dc-link capacitor. |
| $g_a$, $g_b$, $g_c$ | FCS-MPC cost functions. |
| $i_s^a$, $i_s^b$, $i_s^c$ | Power grid phase currents. |
| $i_L^a$, $i_L^b$, $i_L^c$ | Load phase currents. |
| $i_c^a$, $i_c^b$, $i_c^c$ | DSTATCOM phase currents. |
| $\hat{i}_c^a$, $\hat{i}_c^b$, $\hat{i}_c^c$ | DSTATCOM phase current predictions. |
| $i_c^{a*}$, $i_c^{b*}$, $i_c^{c*}$ | DSTATCOM phase current references. |
| $v_c^a$, $v_c^b$, $v_c^c$ | DSTATCOM phase voltages. |
| $n_c$ | Number of cells. |
| $P_c^*$ | Instantaneous active power reference. |
| $Q_c^*$ | Instantaneous reactive power reference. |
| $Q_L$ | Instantaneous reactive load power. |
| $\mathbf{T}$ | Clarke's transformation matrix. |
| $T_s$ | Sampling time. |
| $V_{\rm dc}$ | dc-link voltage. |

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## 1. INTRODUCTION

For today's AC power distribution system, power quality problems play an increasingly important role. This is mainly due to the growth of the electricity demand in the residential and industrial sectors. Recently, poor power quality has become a more important issue for both power suppliers and customers. From a practical point of view, a power quality problem can be defined as a deviation of magnitude and frequency from the ideal sinusoidal waveform. This deviation usually affects both voltage and currents in the distribution systems. These power quality problems have given rise to different developments and these problems have been addressed in the literature from complementary aspects, depending on the type of compensation. Among these developments using for mitigation of power quality issues in the distribution system, it is possible to find the custom power devices (CPDs) based on distribution static compensation (DSTATCOM) are commonly used for reactive power compensation, harmonic mitigation and balancing of source currents [1],[2]. Additional devices such as a dynamic voltage restorer (DVR) is used to compensate unbalance voltage disturbance and a unified power quality conditioners (UPQCs) is used to compensate both, voltage and current quality problems [3],[4].

Moreover, in power quality applications, regardless of the implemented compensation system, the voltage source converters (VSCs) are considered a fundamental element of the compensation systems. A conventional two-level VSC has so far been the most widely used converter in DSTATCOMs however it creates a poor harmonic profile, leading to additional power quality and loss issues [5],[6]. In recent years, the multilevel converter (more than two-level) has drawn the attention of

researchers and the literature has reported the development of DSTATCOMs based on multilevel converter injecting current at the point of common coupling (PCC) in order to achieve the desired reactive power compensation [7],[8]. Regarding the multilevel converter topology, the cascade H-Bridge (CHB) is currently one of the greatest topologies due to its advantages, such as the modular converter topology (which simplifies the increase in the number of levels of the converter) and it does not require a very large number of clamping diodes or flying capacitors [9]. Due to these advantages, the CHB DSTATCOM is now considered as a very competitive topology in the new generation of reactive power compensation devices [10]. Commonly the DSTATCOM based on CHB multilevel converter has been designed using IGBTs power electrics devices but, recently, the SiC-MOSFET devices have gained the focus of researchers because these devices can reach high switching frequencies, far higher to what could be achieved with a multilevel converter based on IGBTs [11],[12]. Nevertheless, for power quality applications using an active power filter, it is not enough to integrate fast switching devices. Rather it is necessary to address this issue together with the control algorithm. In this regard, this paper presents the experimental validation of DSTATCOM based on the SiC-MOSFET CHB multilevel converter for reactive power compensation. This technology uses a fixed switching frequency model-based predictive controller (FSF-MPC) based on a pulse-width modulation strategy [13],[14]. The rest of the paper is divided as follows. Next section introduces the proposed DSTATCOM topology. In the same section, the three-phase 7-level CHB converter scheme is analyzed and the mathematical model of the DSTATCOM based on three-phase 7-level converter and load are extracted. In section 3, the proposed FSF-MPC strategy is detailed. In section 4, the experimental results are shown in which two figures of merits were used as a reference, the current tracking, and reactive power compensation. Finally, in section 5, conclusions of the work are given.

## 2. PROPOSED DSTATCOM TOPOLOGY

Fig. 1 shows the 7-level three-phase CHB multilevel converter. Notice that each cell of the CHB has an independent dc-link and four switching devices based on the SiC-MOSFETs [15]. The 7-level three-phase converter topology is implemented connecting three cells in series per phase. Then, thirty-six firing signals, represented by $S^{\phi}_{xy}$ are used to control each cell, being $\phi$ the phase ($\phi = a$, $b$ or $c$), $x$ the cell number in each phase and $y$ the switching device in each cell ($y = 1$, 2, 3 or 4). Table I shows some combination of the firing signal taking phase "$a$" as an example in order to generate seven voltage levels at the output of the 7-level converter. A similar analysis can be extended to other phases considering allowed combinations and avoid short circuits in the dc-link of each cell.

On the other hand, the control scheme of the proposed FSF-MPC for the DSTATCOM is shown in Fig. 2. This controller is based on the explicit DSTATCOM mathematical model in order to calculate the effects of control actions over the evolution of the states. The dynamic of the system's model can be obtained by using Kirchhoff's circuit laws. Notice that the DSTATCOM based on the CHB 7-level converter is connected at the PCC. Next, by applying Kirchhoff's laws for the AC side of the DSTATCOM, the following equations in the state-space representation are obtained:

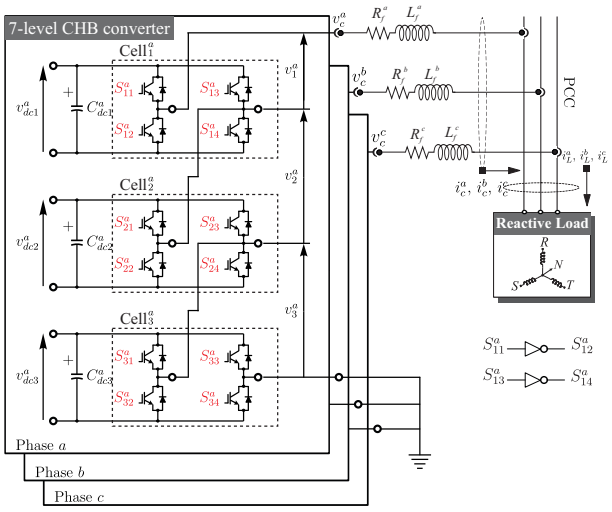


Fig. 1. Three-phase 7-level cascade H-Bridge multilevel converter.

TABLE I
POSSIBLE COMBINATIONS OF ACTIVATION SIGNALS

| $S_\eta^a$ | | | | | | $\eta$ | $v_{c,\eta}^a$ |
|---|---|---|---|---|---|---|---|
| Cell$_1^a$ | | Cell$_2^a$ | | Cell$_3^a$ | | | |
| $S_{11}^a$ | $S_{13}^a$ | $S_{21}^a$ | $S_{23}^a$ | $S_{31}^a$ | $S_{33}^a$ | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | $0{\cdot}v_{dc}^a$ |
| 0 | 0 | 0 | 0 | 0 | 1 | 2 | $-1{\cdot}v_{dc}^a$ |
| 0 | 0 | 0 | 0 | 1 | 0 | 3 | $1{\cdot}v_{dc}^a$ |
| . | . | . | . | . | . | . | . |
| 0 | 1 | 0 | 1 | 0 | 0 | 21 | $-2{\cdot}v_{dc}^a$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 22 | $-3{\cdot}v_{dc}^a$ |
| . | . | . | . | . | . | . | . |
| 1 | 0 | 1 | 0 | 1 | 0 | 43 | $3{\cdot}v_{dc}^a$ |
| . | . | . | . | . | . | . | . |
| 1 | 0 | 1 | 0 | 1 | 1 | 44 | $2{\cdot}v_{dc}^a$ |
| . | . | . | . | . | . | . | . |

$$\begin{bmatrix} \dot{i_c^a}(t) \\ \dot{i_c^b}(t) \\ \dot{i_c^c}(t) \end{bmatrix} = \mathbb{F}. \begin{bmatrix} i_c^a(t) \\ i_c^b(t) \\ i_c^c(t) \end{bmatrix} + \mathbb{G}. \begin{bmatrix} v_s^a(t) - v_c^a(t) \\ v_s^b(t) - v_c^b(t) \\ v_s^c(t) - v_c^c(t) \end{bmatrix} \quad (1)$$

where

$$\mathbb{F} = \begin{bmatrix} -\frac{Rf}{Lf} & 0 & 0 \\ 0 & -\frac{Rf}{Lf} & 0 \\ 0 & 0 & -\frac{Rf}{Lf} \end{bmatrix}, \mathbb{G} = \begin{bmatrix} \frac{1}{Lf} & 0 & 0 \\ 0 & \frac{1}{Lf} & 0 \\ 0 & 0 & \frac{1}{Lf} \end{bmatrix} \quad (2)$$

being $R_f$ the parasitic (series) resistance of the inductive filter $L_f$ connected between the output of the multilevel converter and the PCC.

### A. *DSTATCOM predictive model*

The predictive model can be obtained from (1) by using a forward-Euler discretization method. Euler's method is the most basic explicit method for numerical integration of ordinary differential equations and consequently carries a low computational burden that benefits the experimental implementation. The DSTATCOM discrete-time model is given by:

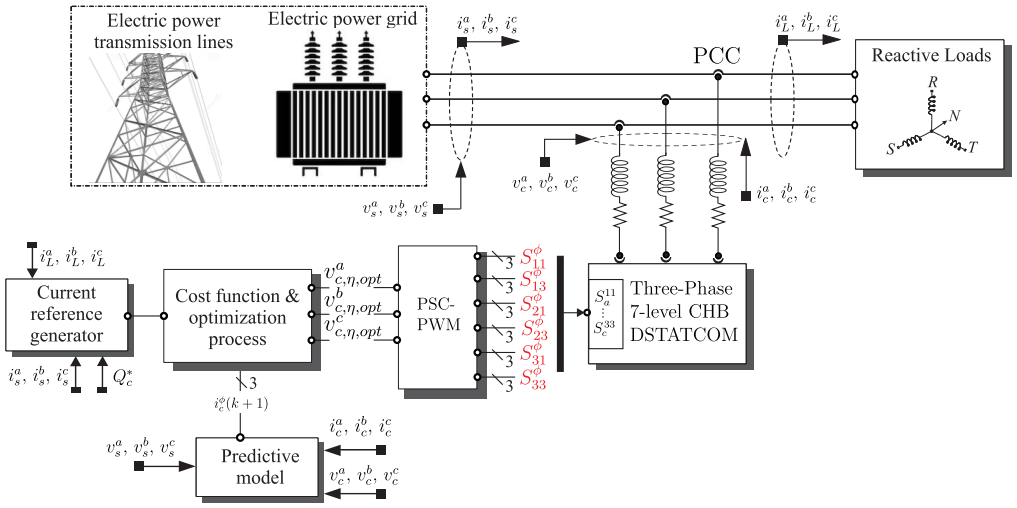


Fig. 2. Control scheme of the proposed FSF-MPC DSTATCOM.

$$\begin{bmatrix} \hat{i}_c^a(k+1) \\ \hat{i}_c^b(k+1) \\ \hat{i}_c^c(k+1) \end{bmatrix} = \mathbb{A}. \begin{bmatrix} i_c^a(k) \\ i_c^b(k) \\ i_c^c(k) \end{bmatrix} + \mathbb{B}. \begin{bmatrix} v_s^a(k) - v_c^a(k) \\ v_s^b(k) - v_c^b(k) \\ v_s^c(k) - v_c^c(k) \end{bmatrix} \tag{3}$$

where

$$\mathbb{A} = \begin{bmatrix} a_1 & 0 & 0 \\ 0 & a_1 & 0 \\ 0 & 0 & a_1 \end{bmatrix}, \mathbb{B} = \begin{bmatrix} \frac{T_s}{Lf} & 0 & 0 \\ 0 & \frac{T_s}{Lf} & 0 \\ 0 & 0 & \frac{T_s}{Lf} \end{bmatrix} \tag{4}$$

being $a_1 = \left(1 - \frac{R_f T_s}{L_f}\right)$ and $T_s$ the sampling time.

### B. *Current reference generation*

The proposed FSF-MPC requires the prior calculation of the reference currents in order to evaluate the cost function in (9). For simplicity, the phase currents and voltages are represented in the $\alpha - \beta$ subspace by using Clarke's transformation matrix:

$$\mathbf{T} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}. \tag{5}$$

Then, the current references in $\alpha - \beta$ subspace in function of active and reactive power are:

$$\begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \end{bmatrix} = \frac{1}{(v_{s\alpha})^2 + (v_{s\beta})^2} \begin{bmatrix} v_{s\alpha} & v_{s\beta} \\ v_{s\beta} & -v_{s\alpha} \end{bmatrix} \begin{bmatrix} P_c^* \\ Q_c^* \end{bmatrix}. \tag{6}$$

In order to achieve unity power factor on the grid side, it must be ensured that $P_c^* = 0$. This condition implies that the DSTATCOM does not absorb active power. On the other hand, the instantaneous reactive power reference can be written as:

$$Q_c^* = -Q_L = v_{s\alpha}\, i_{L\beta} - v_{s\beta}\, i_{L\alpha} \tag{7}$$

where $Q_L$ is compensated by the CHB DSTATCOM system. The DSTATCOM phase currents references used in the optimization process are:

$$\begin{bmatrix} i_c^{a^*} \\ i_c^{b^*} \\ i_c^{c^*} \end{bmatrix} = \mathbf{T}^{-1} \begin{bmatrix} i_{c\alpha}^* \\ i_{c\beta}^* \\ 0 \end{bmatrix}. \tag{8}$$

### C. *Cost function and optimization process*

The proposed controller is based on the model predictive current control. The MPC is based on the optimization process in which a cost function is minimized. This cost function is defined as the difference between reference currents and the predicted currents obtained through the prediction model. In the three-phase control scheme, the cost functions are evaluated independently from the following equations:

$$\begin{aligned} g^a &= \| \, i_c^{a^*} - \hat{i}_c^a(k+1) \, \|^2 \\ g^b &= \| \, i_c^{b^*} - \hat{i}_c^b(k+1) \, \|^2 \\ g^c &= \| \, i_c^{c^*} - \hat{i}_c^c(k+1) \, \|^2 . \end{aligned} \tag{9}$$

Next, the optimization algorithm selects the optimum vector $S_{\eta,opt}^{\phi}$ for each firing signal of each cell by the evaluation and minimization of the predefined cost function represented by (9). To make the thing clearer, Algorithm 1 summarizes the optimization process.

**Algorithm 1** Optimization algorithm of the proposed modulated FSF-MPC current controller

1. Initialize $g_{opt}^a := \infty, g_{opt}^b := \infty, g_{opt}^c := \infty, \eta := 0$
2. Compute the STATCOM current references (8).
3. **while** $\eta \leq \varepsilon$ **do**
4. $\quad S_\eta^\phi \leftarrow S_{xy}^\phi \; \forall \; x \;\&\; y = 1,\ 2,\ 3$
5. $\quad$ Calculate the STATCOM prediction currents (3).
6. $\quad$ Compute the cost function, (9).
7. $\quad$ **if** $g^a < g_{opt}^a$ **then**
8. $\quad\quad g_{opt}^a \leftarrow g^a, \quad S_{opt}^a \leftarrow S_\eta^a$
9. $\quad$ **end if**
10. $\quad$ **if** $g^b < g_{opt}^b$ **then**
11. $\quad\quad g_{opt}^b \leftarrow g^b, \quad S_{opt}^b \leftarrow S_\eta^b$
12. $\quad$ **end if**
13. $\quad$ **if** $g^c < g_{opt}^c$ **then**
14. $\quad\quad g_{opt}^c \leftarrow g^c, \quad S_{opt}^c \leftarrow S_\eta^c$
15. $\quad$ **end if**
16. $\quad \eta := \eta + 1$
17. **end while**
18. Compute the modulation signals (10).
19. Get the turn-on times of the firing signals according to Fig. 3.
20. Apply the firing signals.

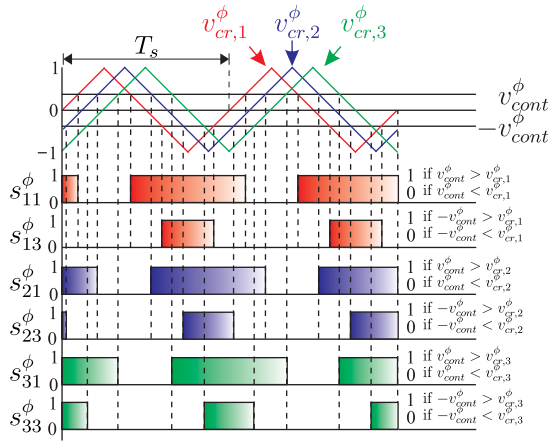


Fig. 3. PSC-PWM scheme for CHB DSTATCOM phase $\phi$.

## 3. PROPOSED FSF-MPC STRATEGY

After selecting the optimal vector $S^{\phi}_{\eta,opt}$, which corresponds to an optimal voltage $v^{\phi}_{c,\eta,opt}$, the classic solution is to apply this output voltage during the whole sampling period. However, the proposed method uses a modulation stage that consists in a phase shift multicarrier pulse width modulation (PSC-PWM). Three phase-shifted triangular carrier waves (with the same frequency and magnitude peak to peak) are needed to obtain the turn-on times of the firing signals of each cell. The phase-shift between the two adjacent carriers is $180^o/3$. By comparing one specific carrier wave $v^{\phi}_{cr,i}$ with a pair of inverted modulation signals $v^{\phi}_{cont}$ and $-v^{\phi}_{cont}$, we obtain the firing signals of $s^{\phi}_{x1}$ and $s^{\phi}_{x3}$, as shown in Fig. 3. Note that the carrier frequency is equal to the sampling frequency and the modulation signals are associated with the optimal phase voltages and are normalized between -1 and 1, that is:

$$v^{\phi}_{cont} = \frac{v^{\phi}_{c,\eta,opt}}{3v_{dc}}. \tag{10}$$

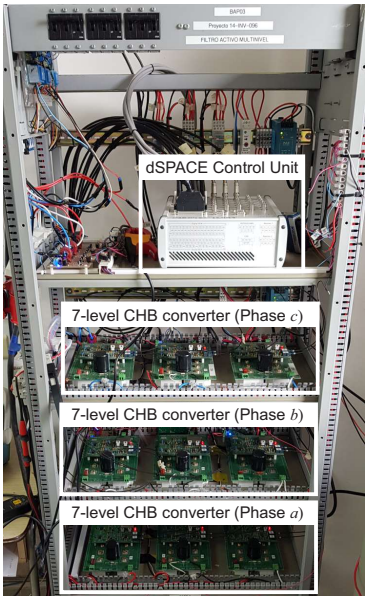


Fig. 4. Block diagram of the DSTATCOM test bench including the 7-level CHB converter, the dSPACE platform and the protection devices.

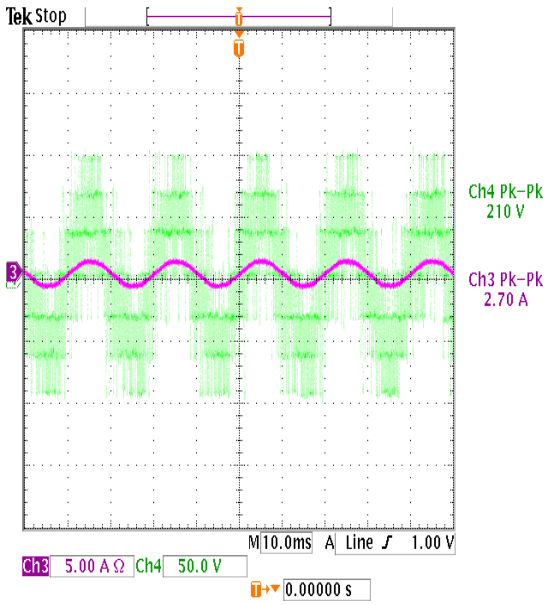


Fig. 5. Voltage at the output of the 7-level converter (before the filter) and load current ($i^a_L$).

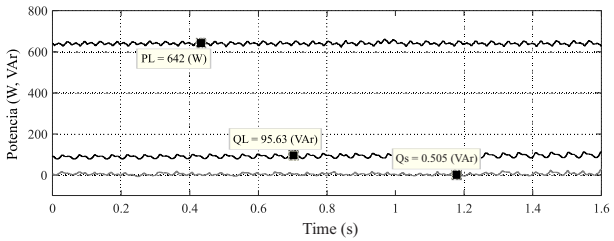


Fig. 6. Experimental result of the reactive power compensation.

## 4. EXPERIMENTAL VALIDATION

The proposed DSTATCOM topology is validated through experimental results obtained by using a custom test bench. This latter integrates three H-Bridge cells per phase that cascaded each other. Each cell is fed with an independent dc-link and integrates four SiC-MOSFET semiconductor devices. The DSTATCOM is controlled by a dSPACE MicroLabBox real-time platform considering a $T_s = 25$ $\mu$s sampling time. The proposed controller is developed by using a MATLAB/Simulink environment. The grid frequency and voltage are set to 50 Hz and 310.2 V, respectively. Other electrical parameters are $v_{\rm dc} = 33$ V, $R_f = 0.09$ $\Omega$, $L_f = 3$ mH, $R_L = 23.2$ $\Omega$ and $L_L = 55$ mH. The experimental measurements of voltage and current are performed with analog meters and are used to validate the proposed control strategy.

Initially, the 7-level CHB converter is analyzed in an open-loop configuration. Fig. 5 shows the seven levels of voltages at the output of the 7-level CHB converter and the load current ($i^a_L$) evolution. Then, the 7-level CHB DSTATCOM is connected at the PCC to perform a dynamic test for the reactive power compensation at the grid side. Fig. 6 shows the results of reactive power compensation. In this test, the active and reactive power at the load side are $Q_L = 95.6$ VAr and $P_L = 642$ W, respectively. As shown in Fig. 6 the reactive power at the grid side is close to zero $Q_S = 0.5$ VAr after the DSTATCOM integration. The reactive power compensation is also verified in Fig. 7 where it shows a unit power factor after the reactive power compensation

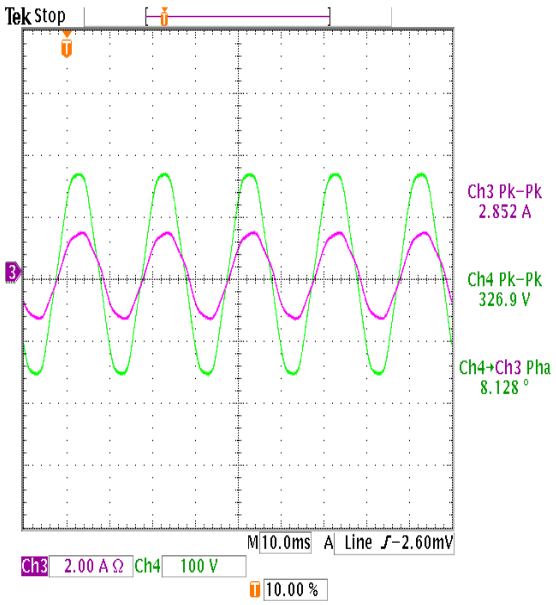


Fig. 7. Voltage ($v_s^a$) and current ($i_s^a$) at the grid side with unit power factor after the reactive power compensation.

at the grid side. This is a zero degree phase shift between the grid voltage ($v_s^a$) and grid current ($i_s^a$). Similar results have been obtained for phases $b$ and $c$ and have not been included for the sake of conciseness.

## 5. CONCLUSION

This paper performs experimental validation of the DSTATCOM based on SiC-MOSFET 7-level converter connected to the point of common coupling in order to maintain nearly unit power factor even when reactive loads are connected to the grid. To accomplish this a control strategy has been proposed based on a fixed switching frequency model-based predictive controller in conjunction with the pulse-width modulation strategy. In this regard, the proposed control scheme fixes the switching frequency from the sampling frequency, which causes a balance in the switching losses in all semiconductor devices. On the other hand, the capability of the 7-level converter has been verified by using the experimental DSTATCOM test bench and it is found to be efficient and robust which is validated through performance under nominal operation, in reactive power compensation.

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