

CMOS Voltage-Controlled Oscillator Resilient Design for Wireless Communication Applications

Ekavut Kritchanchai

Jiann-Shiun Yuan

Department of Electrical Engineering and Computer Science
University of Central Florida
Orlando, Florida 32816, U.S.A.
Email: ekavut1@knights.ucf.edu, jiann-shiun.yuan@ucf.edu

Abstract: Semiconductor process variation and reliability aging effect on CMOS VCO performance has been studied. A technique to mitigate the effect of process variations on the performances of nano-scale CMOS LC-VCO is presented. The LC-VCO compensation uses a process invariant current source. VCO parameters such as phase noise and core power before and after compensation over a wide range of variability are examined. Analytical equations are derived for physical insight. ADS and Monte-Carlo simulation results show that the use of invariant current source improves the robustness of the VCO performance against process variations and device aging.

Key words – Aging effect, phase noise, core power, process variation, LC-VCO

1. INTRODUCTION

With aggressive scaling of CMOS, the controllability of the fabrication process is decreasing with each technology node, especially in the nanometer regime. Negative biased temperature instability (NBTI) and hot carrier injection (HCI) are well-known aging phenomena that degrade transistor and circuit performance. As the characteristic dimensions of device becomes smaller and smaller, it becomes harder and harder to precisely control the physical dimensions and dopant levels during the fabrication process. As a result, these growing uncertainties lead to more and more statistic variations in circuit performance and behaviors from designed circuit. The process variation has been treated mainly as die to die variation, that is the difference originated from different die environments, but devices from the same die share the same properties. With the device size shrinks, intra-die variations have become the main concern for design since it will cause local mismatch even if chips are cut from the same die. Yield analysis and optimization, which takes into account the manufacturing tolerances, model uncertainties, variations in the process parameters, and aging factors are known as indispensable components of the circuit design procedure. The intrinsic device parameter fluctuations that result from process uncertainties have substantially affected the device characteristics. Process variability comes from random dopant fluctuation (RDF), line edge roughness (LER), and poly gate granularity (PGG) [1], [2]

Recently, numerous papers on reliability and process variability and their impact on circuit performances have been published [3]–[7]. For example, NBTI is a major

contributor to CMOS ring oscillator propagation delay [3]. GOB reduces the static noise margin of the SRAM cell [4]. Hot electron effect increases noise figure of low noise amplifier [5], decreases the output power and power efficiency of power amplifier [6], and increases phase noise of cross-coupled oscillator [7]. For process variability, Li et al. [8] studied random-dopant-induced variability in nanoscale device cutoff frequency and CMOS inverter gate delay. Hansson and Alvandpour [9] showed that the delay variation in the master–slave flip flops is 2.7 times larger than the delay variation in a 5-stage inverter chain. Mukhopadhyay et al. [10] presented that large variability and asymmetry in threshold-voltage distribution due to random dopant fluctuation significantly increase leakage spread and degrade stability of fully depleted SOI SRAM cell. Rao et al. [11] described a complete digital on-chip technique to measure local random variation of FET current. Didac Gómez [12] presented a circuit compensation technique to analyze and reduce temperature and process variation effects on low noise amplifiers and mixers. Liu and Yuan [13] developed an adaptive body bias technique for power amplifier resilient to reliability aging and process variations. Han et al. [14] addressed a post-manufacturing self-tuning technique that aims to compensate for multi-parameter variations.

In this work, the reliability and process variability on the RF VCO has been examined. Section II describes the analytical modeling of phase noise and noise factor accounting for device parameter shift resulting from aging. Section III presents the reliability and variability insight of VCO performance before and after current compensation through circuit simulation. Impact of process variations on VCO is evaluated using Monte Carlo simulation. Finally, the conclusion is given in Sec. IV.

2. CIRCUIT ANALYSIS

Both the fabrication process-induced fluctuation and time-dependent degradation cause the MOSFET model parameter to drift. The threshold voltage and mobility are the two most significant model parameters that suffer from process uncertainty and reliability degradations. Here, the most widely used LC-VCO structure in Fig. 1 is used to evaluate the process variations and aging effects on RF VCO performance. The LC-VCO is one of the most important building

blocks in the implementation of a single radio chip in today's various wireless communication systems. LC-VCO is commonly used in CMOS radio frequency integrated circuits because of their good phase noise characteristics and their ease of implementation.

The architecture of LC-VCO uses a cross-coupled pair of NMOS transistors.

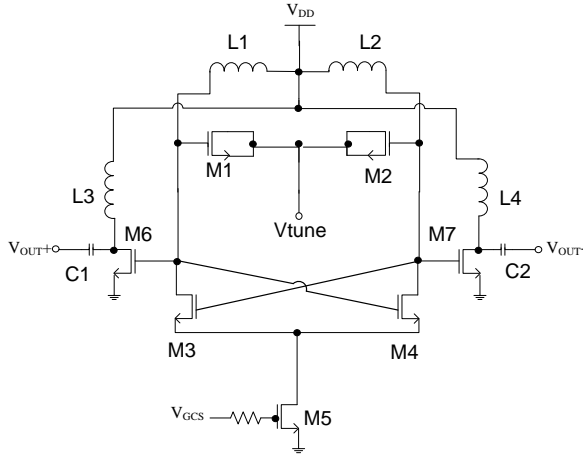


Fig. 1 Schematic of a LC-VCO

Transistor M1 and M2 are used as capacitors. The drain and source terminal are connected to each other and a tuning voltage is applied to that connection. Transistor M3 and M4 are a NMOS cross-coupled pair of the VCO. The transistor M5 provides the bias current. Transistor M6 and M7 are used as a buffer and they produces the output signal

There are many important parameters used to show the performance of the VCO. Phase noise and power consumption are chosen to evaluate the performance of LC-VCO in this paper. Normally, phase noise (L) is characterized by the ratio of phase noise power compared to the signal power. In general, larger signal can be achieved by increasing the core current at the cost of larger power consumption. The output voltage swing of LC oscillator is limited by the saturation conditions of the cross-coupled transistors. When this saturation condition is met, a further increase of the core current will have no effect.

The phase noise of the VCO can be derived as

$$L = \frac{4FkTR}{V_o^2} \left(\frac{\omega_o}{2Q\omega_m} \right)^2 \quad (1)$$

where F is the noise factor, k is the Boltzman constant, ω_o is the carrier center frequency, ω_m is the carrier offset frequency, T is temperature, R is output resistor, Q is the resonator and V_o is the output voltage. The noise factor (F) of the VCO is given by

$$F = 2 + \frac{8\gamma R I_{bias}}{\pi V_o} + \frac{8\gamma g_m R}{9} \quad (2)$$

where γ is the noise factor of single transistor and g_m is the transconductance.

The sensitivity of the LC-VCO can be examined. The process variation and the aging effect may degrade the VCO performance. The Phase noise variation is modeled by the fluctuation of g_m and bias current drift as

$$\Delta F = \frac{\partial F}{\partial g_m} \Delta g_m = \frac{\partial F}{\partial g_m} \left(\frac{\partial g_m}{\partial V_T} \frac{\partial V_T}{\partial I_{bias}} + \frac{\partial g_m}{\partial \mu_n} \frac{\partial \mu_n}{\partial I_{bias}} \right) \Delta I_{bias} \quad (3)$$

where μ_n is the mobility and V_T is the threshold voltage. Expanding the partial derivatives in (3) the phase noise variation can be written as

$$\Delta F = \frac{\gamma 8R}{9} \left\{ \frac{I_{bias}}{(V_{GSOSC} - V_T)^2} \frac{L}{\mu_n C_{ox} W_{CS} (V_{GSOSC} - V_T)} + \frac{I_{bias}}{\mu_n (V_{GSOSC} - V_T)} \frac{2L}{C_{ox} W_{CS} (V_{GSOSC} - V_T)} + \frac{9}{\pi V_o} \right\} \Delta I_{bias} \quad (4)$$

where C_{ox} is the oxide capacitance per unit area, L is the channel length and W is the channel length of the current source transistor, V_{GSOSC} is the gate-source voltage to the cross coupled transistor, and V_{GSOSC} is the gate-source voltage to the current source transistor.

Eq. (4) accounts for process variations and aging effect of the mixer.

It is clear from (4) that the VCO performance is dependent on the drain current of current source. To maintain the mixer performance, the drain current of M5 has to be kept stable. Thus, process invariant current source circuit shown in Fig. 2 is employed. In Fig. 2 drain currents of M8 and M9 are designed the same. Changes in M8 and M10 drain currents are negatively correlated to remain a stable bias current ($I_{D8} + I_{D10}$). For example, if the process variation increases the threshold voltage, but decreases the drain current of M8, the gate voltage of M10 increases ($V_{G10} = V_{DD} - I_{D9}R$). Thus, the drain current of M10 increases to compensate the loss of I_{D8} .

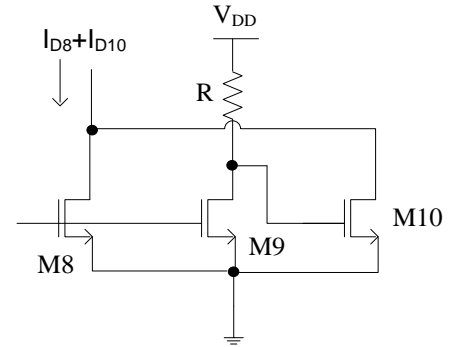


Fig. 2 Process insensitive current source

3. RESULTS AND DISCUSSION

ADS simulation is used to compare the VCO performance using the single transistor current source versus process invariant current source. The RF VCO is operated at 2.4 GHz. The output spectrum is shown in Fig. 3. The output spectrum of the VCO is very peaked near the oscillation frequency (2.4GHz).

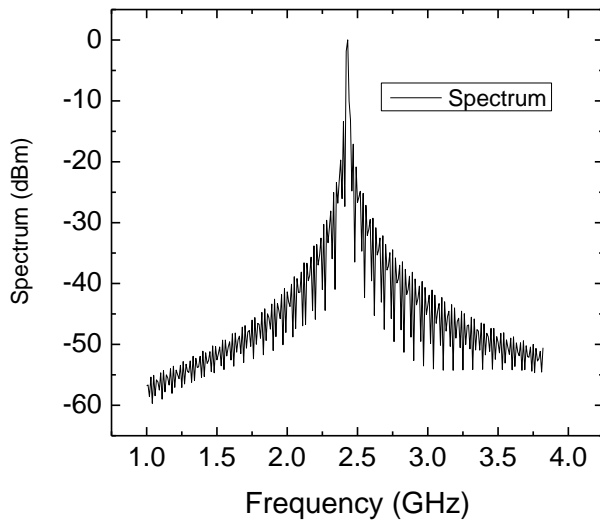


Fig. 3 The output spectrum

In the circuit design, CMOS 0.18 μm mixed-signal technology node is used. L1 to L4 are chosen at 2nH. The transistor channel widths of M1 and M2 are 696 μm . The channel widths of M3 and M4 are 128 μm . The channel width of M5 is 300 μm . The channel widths of M6 and M7 are 48 μm . The gate resistor size of the current source is 200 Ω . The mixer sets the gate biasing voltage at the current source at 0.9 V. In the current source, the transistor M8 and M9 match each other as 100 μm . The width of M10 is 600 μm . The supply voltage V_{DD} is 1.8 V. The tuning voltage is 0.5 V.

For the process variation effect, the phase noise of the VCO is evaluated at 1MHz offset frequency using different process corner models and variable resistance due to inter-die variations. One naming convention for process corner models is using two-word designators, where the first word refers to the N-channel MOSFET (NMOS) corner, and the second word refers to the P channel (PMOS) corner. In this naming convention, three corner models exist: typical, fast and slow. Fast and slow corners exhibit carrier mobilities that are higher and lower than normal, respectively. The simulation result of the (ff), (ss), (sf), (fs), and (tt) is shown in Fig. 4(a). It is clear from Fig. 4(a) that the VCO with the invariant current source shows robust phase noise against different process variations.

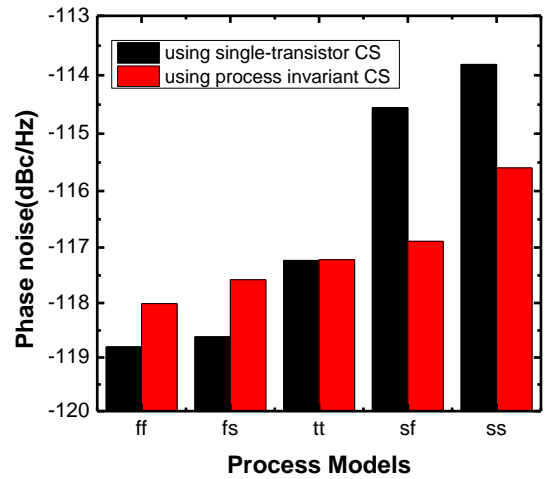


Fig. 4(a) Phase noise by different process models

The phase noise gain is also evaluated using different threshold voltage and mobility degradations resulting from aging (hot carrier effect) as shown in Figs. 4(b) and 4(c). The hot-carrier injection increases the threshold voltage, but decreases the electron mobility. The phase noise increases with an increased threshold voltage or decreased mobility due to reduced transconductance. Again, the VCO with process invariant current source exhibits more robust performance against threshold voltage increase and mobility degradation.

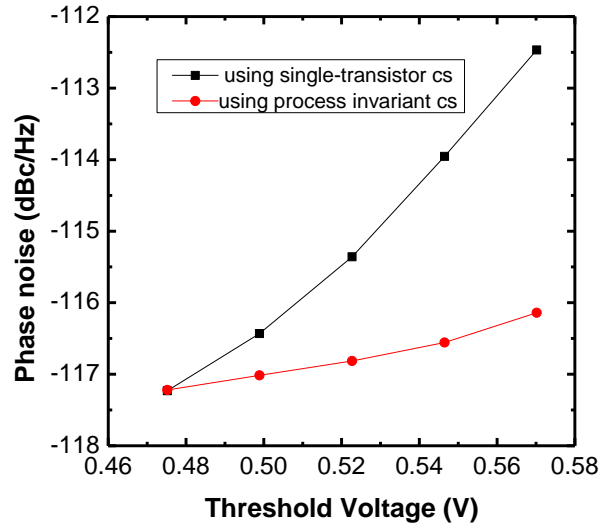


Fig. 4(b) Phase noise versus threshold voltage

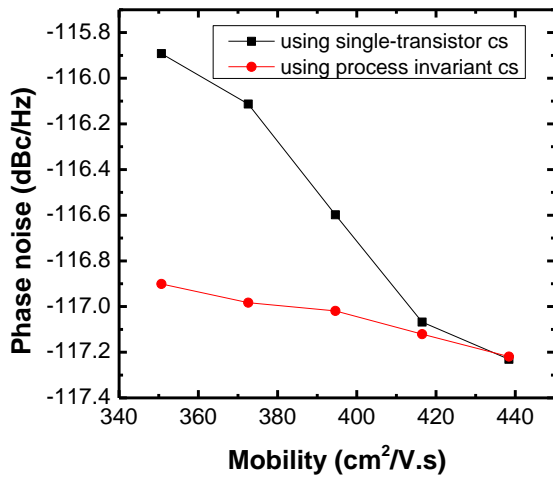


Fig. 4(c) Phase noise versus electron mobility

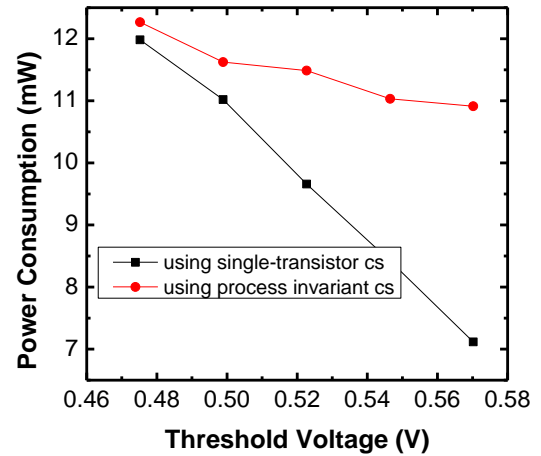


Fig. 5(b) Power consumption versus threshold voltage

In addition, the power consumption of the VCO using the process invariant current source is compared with that using the single transistor current source. The power consumption versus different process models is displayed in Fig. 5 (a). It is clear from Fig. 5(a) that the power consumption is more stable over different corner models for the mixer using the current invariant current source. The power consumption also shows less threshold voltage and mobility sensitivity as evidenced in Figs. 5(b) and 5(c). In Figs. 5(b) and 5(c) the power consumption decreases with increased threshold voltage and decreased mobility due to reduced drain current and transconductance in the VCO.

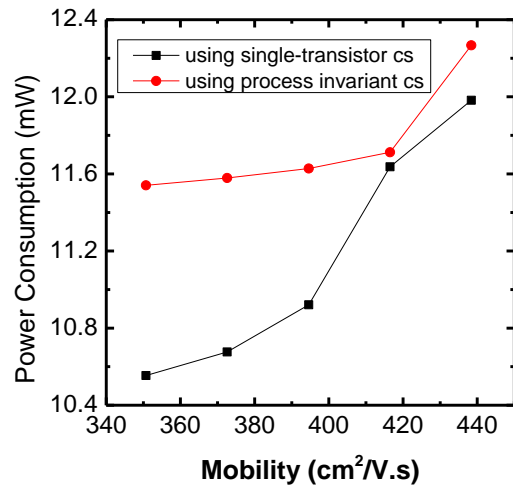


Fig. 5(c) Power consumption versus electron mobility

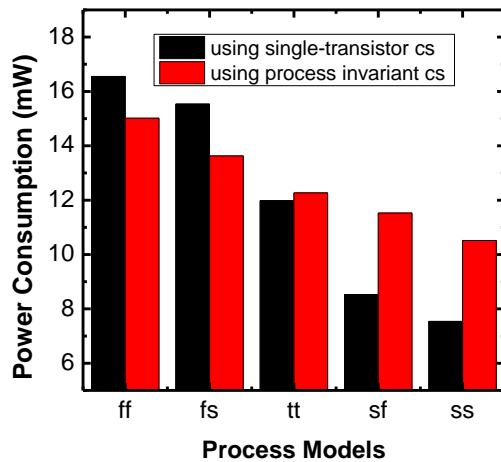


Fig. 5(a) Power consumption predicted using different process models

To further examine the process variation and reliability impact on RF LC-VCO, Monte-Carlo (MC) circuit simulation has been performed. In ADS the Monte-Carlo simulation assumes statistical variations (Gaussian distribution) of transistor model parameters such as the threshold voltage, mobility, and oxide thickness. In the Monte-Carlo simulation a sample size of 1000 runs is adopted. Figs. 6 (a) and 6 (b) display the histograms of phase noise using single transistor current source (traditional) and using the process invariant current source (after compensation). For the mixer using the traditional current source, the mean value of phase noise is -117.06 dBc/Hz and its standard deviation is 1.48%. When the process invariant current source is applied, the mean value of phase noise changes to -117.29 dBc/Hz and its standard deviation reduces to 0.34%.

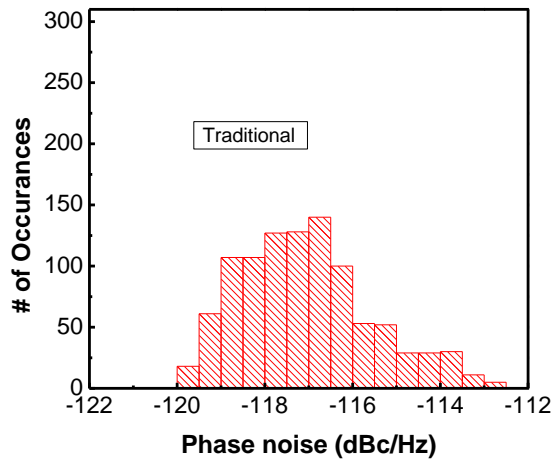


Fig. 6(a) Phase noise statistical distribution without compensation

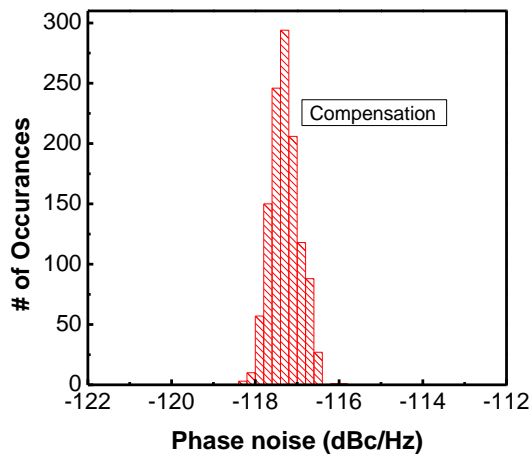


Fig. 6(b) Phase noise statistical distribution after process compensation effect

4. CONCLUSION

Semiconductor process variations and hot electron reliability on the LC-VCO performance have been evaluated using different process models and key model parameters such as threshold voltage and mobility. The phase noise and power consumption show robust performance for the VCO using the process invariant current source compared to that using the traditional single transistor current source. Monte-Carlo simulation demonstrates that the standard deviation of phase noise reduces from 1.48% to 0.34% while their relative mean values remain the same.

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